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- (71) Applicant (for all designated States except US): **AOTI OPERATING COMPANY, INC.** [US/US]; 131 NW Hawthorne Avenue, Suite 207, Bend, OR 97701 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **SMITH, Nigel, Peter** [GB/GB]; Accent Optical Technologies, Haxby Road, York YO31 8SD (GB). **HAMMOND, Michael, John** [GB/GB]; Accent Optical Technologies, Haxby Road, York YO31 8SD (GB).
- (74) Agent: **NOVAGRAAF PATENTS LIMITED**; The Crescent, 54 Blossom Street, York YO24 1AP (GB).
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(54) Title: **OVERLAY METROLOGY MARK**

(57) Abstract: An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with and in particular developed on a first layer and a second mark portion associated with and in particular developed on the surface of a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal array of individual test structures. A method of marking and a method of determining overlay error are also described.